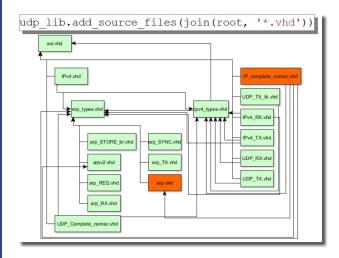
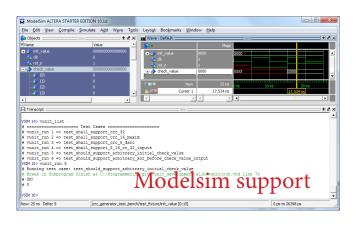
## VUnit A Unit lesting work for VHDL **A Unit Testing Frame-**

A tool suite to improve VHDL testing through automation



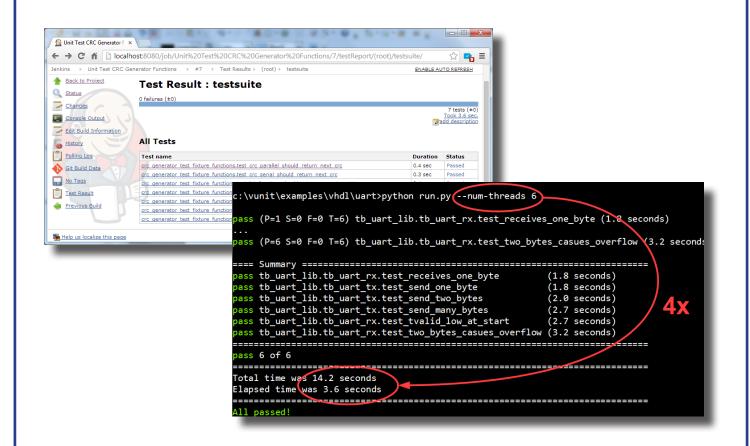
- Free and open source: https://github.com/LarsAsplund/vunit
- Active and responsive community
- Increases productivity by enabling early and frequent testing through automation: https://www.youtube.com/watch?v=PZuBqcxS8t4
- Scanners for identifying files, tests, file dependencies, and file changes enable for automatic (re)compilation and execution of test suites
- Multithreading for increased test performance
- Scripting as well as command line support
- Python test runner that enables powerful test administration, can handle VHDL fatal runtime errors (e.g. division by zero), and ensures test case independence
- Support for running same test suite with different generics
- Assertion checker library that extends VHDL built-in support (assert)
- Feature rich logging framework
- Message passing mechanism for high-level testbench communication





- ModelSim and GHDL fully supported. Rivera-PRO and Active-HDL with full support in Q3-15.
- Support for both Windows and Linux
- Support for VHDL-93, 2002, and 2008
- JUnit report files for better Jenkins integration





## **Synective Labs - The FPGA Experts**

Synective Labs is specializing in FPGA technology and FPGA based solutions with focus on high performance systems. Our offerings range from development of complete systems to assisting in our cutomers development process, helping them to design better products. With VUint we have helped customers to with less effort increase test coverage and quicker reach fully functional systems. How can we help you?



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