



Features

- Multiple Channels**
- Low-Latency DMA with Interrupt Rate Adaption**
- Small Size**
- System Bus Interface**
- Option to Use Only Core Logic**
- Timestamps**
- Bus Load Calculation**
- Status Updates in Data Stream**
- Separate System Bus and Core Clocks**
- Configurable Hardware Buffer Size**
- Transmit Rate Limit**
- Listen Only-mode**
- Interrupt Logic**
- CAN FD, both ISO and non-ISO**
- CAN 2.0A and 2.0B**

In Short

CAN (Controller Area Network) is a multicast multi-master serial bus commonly used in automotive and industrial applications. Our IP conforms to the CAN FD (Flexible Data-Rate) supports standard CAN bus speeds between 1 kbit/s to 1Mbit/s and CAN FD data phase bit rates at 3 clock cycles per bit reaching 13.333... Mbit/s with a 40 MHz clock.

The IP may be configured to contain multiple CAN cores. These will share a receive buffer and timestamp counter, potentially saving precious resources. Data can be transferred to the host system either by reading the shared receive buffer, or using its low-latency DMA solution.

The IP is delivered as a system bus interfaceable core bundled with demo software to allow for easy integration. The bus type varies between platforms.

It is also possible to directly interface the BSP (Bit Stream Processor) block. This is the core module of the IP, stripped of buffers and many features, thus making it very small. Approximate resource usage is 1,100 4-input LUTs and 330 registers.

Sample Build Sizes

The IP has been designed to have a small resource usage. Approximate build results for a few different settings are shown in the table below.

Setup	4-input LUTs	Registers
CAN core, RX buffer	2,400	1,200
CAN core, RX buffer with DMA	2,500	1,300
CAN core, RX buffer with DMA, Timestamps	2,700	1,600
CAN core, RX buffer with DMA, Timestamps, Bus synchronization	2,900	1,800